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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09 872,798	06 02 2001	Hirofumi Harada	S004-4310	4143

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ADAMS & WILKS
ATTORNEYS AND COUNSELORS AT LAW
31st FLOOR
50 BROADWAY
NEW YORK, NY 10004

EXAMINER

LE, THAO X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 11/29 2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,798

Applicant(s)

HARADA, HIROFUMI

Examiner

Thao X Le

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A2

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 10-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 10-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Acknowledgement

1. Applicant's cancellation of claims 2-9 in Paper No. 8 is acknowledged.

Specification

2. Claim 1 is objected to because of the following informalities: In claim 1 line 21, 'a second gate comprises....'. It is suggested to change to 'a second gate material....'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 19-20 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Recited claim 19 '...further comprising a source electrode connected to the semiconductor substrate' which is not disclosed in the specification. Claim 20 is rejected at least as being depended on claim 19.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

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(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 10-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6117734 to Nakamura.

Regarding to claim 1, Nakamura discloses a vertical MOS transistor in fig. 22 comprising: a semiconductor substrate 1b having a first conductivity type, a body region 2, an epitaxial growth layer 1 having the first conductivity type formed on the semiconductor substrate 1b, a body region 2 having a second conductivity type formed on the epitaxial growth layer 1, a trench 4, fig. 1, column 7 line 38, formed through body region of a second conductivity type so as to reach inside of the epitaxial growth layer 1 of the first conductivity type, a gate insulating film 9, column 7 line 47, formed along an upper surface of the body region 2 of second conductivity type and a wall surface and a bottom surface of the trench, a polycrystalline silicon gate 22, column 9 line 13, partially filling the trench 4 so as to be in contact with the gate insulating film 9 and surrounded by the gate insulating film 9, a second gate material 11 comprises one of a silicon oxide film, column 11 line 13, filling a remaining portion of the trench not filled by the polycrystalline silicon gate, so as to be in contact with the polycrystalline silicon gate 22 and surrounded by the gate insulating film 9 and polycrystalline silicon gate 11 (further surrounded detail can be seen in fig. 5c), a source region 2 of first conductive type formed in the upper surface of the body region of second conductivity type and around trench so as to be in contact with the gate insulating film 9, a gate electrode connected to the polycrystalline silicon

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gate and the second gate material, a source electrode 14a connected to the source region, a drain electrode 14c connected to the semiconductor substrate.

Regarding to claim 10, Nakamura discloses a vertical MOS transistor in fig. 22 comprising: a semiconductor substrate 1b having a first conductivity type, a body region 2, an epitaxial layer 1 having the first conductivity type formed on the semiconductor substrate 1b, a body region 2 having a second conductivity type formed on the epitaxial growth layer 1, a trench 4, fig. 1, column 7 line 38, extending through at least the body region and extending into the epitaxial growth layer 1, a gate insulator film 9, column 7 line 47, formed in the trench, a gate 22, column 9 line 13, formed of a first gate material disposed in the trench 4 so as to be surrounded by the gate insulator 9 and a second gate material 11 comprised of an insulating material, column 11 line 13, disposed in the trench so as to be surrounded by the gate insulator 9 and first gate material (further surrounded detail can be seen in fig. 5c).

Regarding to claims 11-14 Nakamura discloses a vertical MOS transistor in fig. 22 wherein the first gate material comprises polycrystalline silicon and the second gate material 11 comprises one of an oxide of silicon oxide, column 9 lines 13-15, wherein the first and second gate materials fill up the trench so that there is substantially no void at a top surface of the gate, wherein the gate insulator 9 is formed of silicon oxide, column 9 line 16, wherein the second material 11 is in contact with the first gate material 22.

Regarding to claims 15-18, Nakamura discloses a vertical MOS transistor in fig. 22 further comprises a source region 3 having the first conductivity type formed in a upper surface of the body region 2 to surround the trench and in contact with the gate insulator, fig. 22, wherein a source electrode 14a connected the source region 3, and drain electrode 14c connected

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to the semiconductor substrate 1b, wherein the trench is formed in a U shape, wherein a body electrode 14a connected to the body region and the source electrode.

Response to Arguments

5. Applicant's arguments with respect to claim 1, 10-18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
November 22, 2002


PHAT N. C.
PRIMARY EXAMINER